Modul – No.		781	Mandatory	
Module name		**Dependable System Design**		
Module coordinator		Prof. Dr. Mario Schölzel		
Title		Dependable System Design		
Title of examination		Dependable System Design		
Semester		1		
Course Type	Language	Lecture including exercises	English	
SWS/ ECTS/ Workload		4	5	150
Requirements for attendance		None		

1. Content and objectives

Content:

The module provides an introduction into techniques, measures, means and standards for designing and developing dependable system:

- Introduction and Terminology: Threats, Means, Meassures
- Fault Models and Fault sources
- Redundancy Concepts and architectures
    - Software-Redundancy
    - Hardware-Redundancy (active/passive)
    - Data Redundancy (error detection codes, error correction codes)
    - Time-Redundancy
- Testing hardware and software
- Modeling and Estimating Reliability and Availability
    - Failure rate
    - Reliability and MTTF
    - Serial-/Parallel Systems
    - RBD, failure-trees
    - Markov-Models
- Functional Safety and ISO 26262

Objectives:

The student has a good knowledge about the terminology for dependability. He knows the threats that affect the dependability of a system negatively as well the means that affect the dependability in a positive way. He can apply these means in different design phases for developing a dependable system. By understanding the models for reliability and availability, the student can justify his design choices for increasing reliability and availability. The student is also ware of standards for developing dependable systems, as an example he knows the ISO 26262 for designing electronic automotive systems.

Recommended Literature:

Kishor S. Trivedi: Probability and Statistics with Reliability, Queuing and Computer Science Applications (Second Edition). John Wiley & Sons, Inc., 2002.

Dhirak K. Pradhan: Fault-Tolerant Computer System Design. Prentice Hall PTR, 1996.

Isreal Koren and C. Mani Krishna: Fault-Tolerant Systems, Morgan Kaufmann, 2007.

Parag K. Lala: Self-Checking and Fault-Tolerant Digital Design.Morgan Kaufmann, 2001.

Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen (Editors): VLSI test Principles and Architectures. Morgan Kaufmann, 2006.

Abramovici, M. Breuer, M., Friedman, A. „Digital Systems Testing and Testable Design" Computer Science Press, 1990,

2. Methods of instructions

Lecture with integrated exercises

3. Requirements for attendance

No course specific requirements.

4. Usability of this module

The module is offered as mandatory course in the master study course „Computer Engineering for IoT Systems" as well as elective course in other master courses of the Engineering Department.

5. Requirements for assessment

Assessment is performed either as written examination (90 minutes) or oral examination. Students need to pass the module examination, which encompasses all contents of the lecture.

6. ECTS credits

5 ECTS credits

7. Frequency of offer

Every summer term

8. Work load

150 h of total work load, from:

- 45 h of presence at lectures/exercises
- 55 h of self-study
- 50 h of preparation for examination

9. Duration of module

1 semester